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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,233	05/11/2001	Steven T. Harshfield	MICS:0061	5984

7590 02/18/2003

Michael G. Fletcher
Fletcher, Yoder & Van Someren
P.O. Box 692289
Houston, TX 77269-2289

EXAMINER

COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 02/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/853,233

Applicant(s)

HARSHFIELD ET AL.

Examiner

W. David Coleman

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-21,23-26,28-33,35-40 and 42-44 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5-13,15-21,23-26,28-33,35-40 and 42-44 is/are rejected.
- 7) ☒ Claim(s) 14 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. The indicated allowability of claims 8-16 is withdrawn in view of the newly discovered reference(s) to Kozicki et al., U.S. Publication No.: US 2002/0168820 A1. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
- (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 23, 24, 25, 26, 28, 29, 30, 31, 32, 33, 35, 36, 37, 38, 39, 40, 42, 43 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozicki et al., U.S. Patent Application Publication No.: US 2002/0168820 A1.

4. Kozicki discloses a semiconductor device as claimed. See **FIGS. 1-29**.

5. Pertaining to claims 1, 8, 11 and 16 Kozicki teaches a memory cell comprising:
 - a first line **100** formed over a substrate, the first line being formed of a first conductive material (i.e., tungsten, nickel, molybdenum, platinum or metal silicides);
 - a layer of a second conductive material **160** disposed over the first line, the second conductive

material being different from the first conductive material (silver iodide);

a layer of chalcogenide material **140** disposed over the layer of the second conductive

material; and

a second line **120** formed over the layer of chalcogenide material.

6. Pertaining to claims 2 and 32, Kozicki teaches the memory cell, as set forth in claim 1, wherein the first line is embedded in the substrate.

Pertaining to claims 3 and 33, Kozicki teaches the memory cell, as set forth in claim 1, wherein the first line is disposed in a window formed in a dielectric layer **150** disposed over the substrate.

7. Pertaining to claims 5 and 12, Kozicki teaches the memory cell, as set forth in claim 1, wherein the layer of a second conductive material is deposited on the first line using an immersion plating technique (please note that there is no patentable weight given to the process since these are product by process claims and only the product will be examined).

8. Pertaining to claims 6 and 13, Kozicki teaches the memory cell as set forth in claim 1, wherein the second conductive material comprises at least one of silver and gold.

9. Pertaining to claims 7 and 20, Kozicki teaches the memory cell as set forth in claim 1, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

10. Pertaining to claim 9, Kozicki teaches the memory cell as set forth in claim 8, wherein the first line is embedded in the substrate.

Art Unit: 2823

11. Pertaining to claim 17, Kozicki teaches the memory cell, as set forth in claim 16, wherein the first line is embedded in the substrate.
12. Pertaining to claim 18, Kozicki teaches the memory cell, as set forth in claim 16, wherein the first line is disposed in a window formed in a dielectric layer disposed over the substrate.
13. Pertaining to claims 21, 24 and 25, Kozicki teaches a memory cell comprising:
 - a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;
 - a first line disposed in the first window, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel and tungsten;
 - a second layer of dielectric material disposed over the first layer of dielectric material and over the first line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;
 - layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;
 - layer of chalcogenide material disposed in the second window over the layer of the second conductive material; and
 - second line formed over the layer of chalcogenide material.

Art Unit: 2823

14. Pertaining to claim 23, Kozicki teaches the memory cell, as set forth in claim 2 1, wherein the layer of a second

conductive material is deposited on the first line using an immersion plating technique.

15. Pertaining to claims 26 and 29, Kozicki teaches a memory cell comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein; a first line disposed in the first window, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel and tungsten;

a second layer of dielectric material disposed over the first layer of dielectric material and over the first line;

first layer of conductive material disposed over the second layer of dielectric material, the first layer of conductive material; and the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first line;

a layer of a second conductive material disposed in the second window over the first line, the second conductive material being different from the first conductive material;

a layer of chalcogenide material disposed in the second window over the layer of the

second conductive material that comprises one of aluminum, copper, nickel and tungsten; and

a second line formed over the layer of chalcogenide material and over the first layer of conductive material.

16. Pertaining to claim 28, Kozicki teaches the memory cell, as set forth in claim 26, wherein the layer of a second

conductive material is deposited on the first line using an immersion plating technique.

17. Pertaining to claim 30, Kozicki teaches the memory cell, as set forth in claim 26, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

18. Pertaining to claim 31, Kozicki teaches a memory comprising:

a memory array having a plurality of memory cells, each of the memory cells comprising:

a first line formed over a substrate, the first line being formed of a first conductive

material that comprises one of aluminum, copper, nickel and tungsten; a layer of a second conductive material disposed over the first line, the second

conductive material being different from the first conductive material;

a layer of chalcogenide disposed over the layer of the second conductive material;

and a second line formed over the layer of chalcogenide.

19. Pertaining to claim 32, Kozicki teaches the memory cell, as set forth in claim 31, wherein the first line is embedded in the substrate.

• Art Unit: 2823

20. Pertaining to claim 33, Kozicki teaches the memory cell, as set forth in claim 31, wherein the first line is disposed in a window formed in a dielectric layer disposed over the substrate.
21. Pertaining to claim 35, Kozicki teaches the memory cell, as set forth in claim 31, wherein the layer of a second conductive material is deposited on the first line using an immersion plating technique.
22. Pertaining to claim 38, Kozicki teaches an electronic device comprising:
 - a processor; a memory operatively coupled to the processor, the memory comprising a memory array having a plurality of memory cells, each of the memory cells comprising:
 - a first line formed over a substrate, the first line being formed of a first conductive material that comprises one of aluminum, copper, nickel and tungsten; a layer of a second conductive material disposed over the first line, the second conductive material being different from the first conductive material;
 - a layer of chalcogenide disposed over the layer of the second conductive material;
 - and
 - a second line formed over the layer of chalcogenide.
23. Pertaining to claim 39, Kozicki teaches the memory cell, as set forth in claim 38, wherein the first line is embedded in the substrate.
24. Pertaining to claim 40, Kozicki teaches the memory cell, as set forth in claim 38, wherein the first line is disposed in a window formed in a dielectric layer disposed over the substrate.

Art Unit: 2823

25. Pertaining to claim 42, Kozicki teaches the memory cell, as set forth in claim 38, wherein the layer of a second conductive material is deposited on the first line using an immersion plating.

Objections

26. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

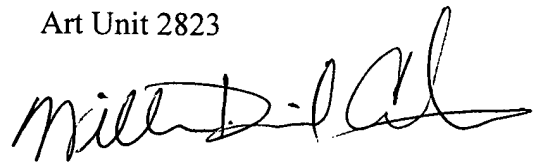
Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W. David Coleman
Examiner
Art Unit 2823



WDC
February 13, 2003